US-PAT-NO: 5965871

DOCUMENT-IDENTIFIER: US 5965871 A

TITLE: Column readout multiplexer for CMOS image sensors with multiple readout and fixed pattern noise cancellation

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Detailed Description Text - DETX (9):
When reset transistor 38 is turned ON by the application of a RESET signal to gate 41, sensing node 36 is clamped to VDD which exerts a reverse bias on photo-diode 34 to induce the depletion. While reverse biased, if photo-diode 34 is illuminated, minority carriers will diffuse into the depletion region causing electrical charge to be stored therein proportional to the light cast thereon. This stored charge represents the image information content of the pixel unit cell. Also, while reset transistor 38 is turned ON, gate 45 of transistor 42 is biased such that a reference potential is provided at the source 47 of row select transistor 44 via transistor 42. When transistor 44 is subsequently turned ON by the application of a row select signal to gate 51, column bus 16 will be pulled up to the reset reference level until transistor 44 is turned OFF.

Detailed Description Text - DETX (16):
The second terminal 77 of second isolating switch 76 is also coupled to the gate 80 of a second source follower transistor 82 which implements reset amplifier 30 (FIG. 1) of readout circuit 22. Transistor 82 includes a drain

coupled to ground and a source selectively coupled to a second output terminal
86 by a second column select switch 84. A second terminal 85 of switch 84 is
also coupled to a second current source 88. Reset reference output terminal 86
provides an analog reset reference output signal COUTR. Current source 88 is
likewise included within analog bias circuit 24 (FIG. 1) and provides a bias
current to the reference output terminal 86 of each of the m readout circuits
22 in APS structure 10 (FIG. 1). A control input (not shown) to second column
select switch 84 is coupled to receive the column select signal CSEL from the
output of timing control circuit 23 (FIG. 1).

Detailed Description Text - DETX (50):
A second current source 198 is coupled between output terminal 200 and
ground. Current source 198 is likewise included within analog bias circuit 24
(FIG. 1) and provides a bias current to the reset output terminal 200 of each
of the m of readout circuits 22 in APS structure 10 (FIG. 1).

Current US Original Classification - CCOR (1):
250/208.1